

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
(Case No. 209.009-US)

In the Application of: **STONICK ET AL.**

Serial No: **10/630,911**

Filed: **JULY 29, 2003**

Title: **RECEIVER BASED DECISION FEEDBACK  
EQUALIZATION CIRCUITRY AND TECHNIQUES**

)  
) Group  
) Art Unit: **2631**  
)  
) Before  
) Examiner

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

I hereby certify that this  
correspondence is being deposited  
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on November 21, 2003

Date  
Michiko Sites  
(person signing this certificate)

Michiko Sites  
Signature

**FIRST INFORMATION DISCLOSURE STATEMENT**

Dear Sir:

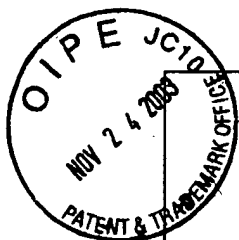
Submitted herewith is one (1) sheet of a modified Form PTO-1449. A copy of each document cited on the attached Form PTO-1449 is also submitted.

It is respectfully requested that the Examiner make his/her consideration of these documents formally of record with the initial Office Action.

Respectfully submitted,

Neil A. Steinberg  
Reg. No. 34,735  
650-968-8079

Date: November 21, 2003



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO.	SERIAL NUMBER
	209.009-US	10/630,911
	APPLICANT(S)	
	Stonick t al.	
	FILING DATE	GROUP ART UNIT
	July 29, 2003	2631

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	2001/0022813	9/2001	Tan et al.			
	2002/0009135	1/2002	Omura et al.			
	2002/0083396	6/2002	Azadet et al.			
	2002/0172276	11/2002	Tan et al.			
	2003/0016770	1/2003	Trans et al.			
	2003/0058955	3/2003	Raghavan			
	2003/0063664	4/2003	Bodenschatz			
	2003/0067865	4/2003	Gross et al.			
	2003/0115541	6/2003	Azadet et al.			
	4,583,234	4/1986	Ramadan			
	6,192,072	2/2001	Azadet et al.			
	6,249,544	6/2001	Azazzi et al.			
	6,252,904	6/2001	Agazzi et al.			
	6,363,112	3/2002	Azadet et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	"A Redundant Multi-Valued Logic for 10Gb/s CMOS Demultiplexer IC", Tanabe et al., ISSCC 2001 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp.220-221, 449-450, 14 slides

EXAMINER	DATE CONSIDERED
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	